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U.S. Department of Commerce, Patent and Trademark Office Serial No. Atty Docket No. M-7086 US 09/347,106 EIVED INFORMATION DISCLOSURE STATEMENT BY APPLICANT **Applicant** (Use several sheets if necessary) Hronik, Stanley A.V. Filing Date July 2, 1999 U.S. Patent Documents Document *Examiner Filing Date Number Class Subclass Initial Date Name If Appropriate Wyland AA 4,882,709 11/21/89 365 189.02 MI AB 5,515,325 05/07/96 Wada 365 189.01 AC 5,526,320 06/11/96 Zagar et al. 365 233.5 AD 5,546,344 08/13/96 **Fawcett** 365 189.05 ΑE 5,568,430 10/22/96 365 189.05 Ting Johnson et al. 71395 AF 5,577,236 11/19/96 400551 5,617,362 04/01/97 Mori et al. 189.05 AG 365 Amini et al. 128 250 AH 5,644,729 07/01/97 110395 ΑI 5,652,724 07/29/97 Manning 365 189.05 71/395 ΑJ 5,659,696 08/19/97 Amini et al. 202412 ΑK 5,663,901 09/02/97 Wallace et al. 365 52 Foreign Patent Documents Translation Yes Document Class Subclass Date Country No ΑL AM AN AO ΑP ART (Including Author, Title, Date, Pertinent Pages, Etc.) Gibson, Glenn A., Computer Systems--Concepts and Design, Prentice Hall, Inc., Englewood Cliffs, New AQ Jersey, 1991, pp. 366-369 and 452-493 Prince, Betty, Semiconductor Memories, Second Edition, (John Wiley & Sons ed., 1991) (1983) pp. 467-AR "64K x 32, 3.3V Synchronous SRAM With Pipelined Outputs and Interleaved/Linear Burst Counter, AS Preliminary IDT71V632," Integrated Device Technology, Inc., Product Information, March 1997, 14 pages Date Considered Examiner *EXAMINER! Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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